JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

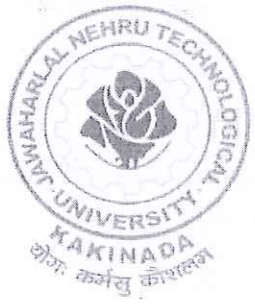
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE M.Tech ECE Common for

I. Digital Electronics & Communication Engineering (DECE)
II. Digital Electronics & Communication Systems (DECS)
III. Electronics & Communication Engineering (ECE)

Programme

(Applicable for batches admitted from 2019-2020)



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

I Semester

S. No.	Course Type/ Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Core 1	Digital System Design	3	0	0	3
2	Core 2	Digital Data Communications	3	0	0	3
3	Prog. Specific Elective	**Elective I** a) Transform Techniques b) VLSI Technology and Design c) Radar Signal Processing	3	0	0	3
4	Prog. Specific Elective	**Elective II** a) Statistical Signal Processing b) Optical Communication Technology c) Network Security & Cryptography	3	0	0	3
5	Lab 1	System Design Using Verilog HDL Lab	0	0	4	2
6	Lab2	Data Communications Lab	0	0	4	2
7		Research Methodology and IPR	2	0	0	2
8	Aud 1	Audit Course 1	2	0	0	0
	Total		**16**	**0**	**8**	**18**

II Semester

S. No.	Course Type/ Code	Name of the Subject	Teaching Scheme			Credits
			L	T	P	
1	Core 3	Image and Video Processing System Design	3	0	0	3
2	Core 4	Wireless Communications and Networks	3	0	0	3
3	Prog. Specific Elective	**Elective III** a) CMOS Analog & Digital IC Design b) Advanced Computer Architecture c) Soft Computing Techniques	3	0	0	3
4	Prog. Specific Elective	**Elective IV** a) DSP Processors and Architectures b) EMI/ EMC c) Object Oriented Programming	3	0	0	3
5	Lab 1	Advanced Communications Lab	0	0	4	2
6	Lab2	Advanced Image processing Lab	0	0	4	2
7	MP	Mini Project(Seminar)	0	0	4	2
8	Aud 2	Audit Course 2	2	0	0	0
	Total		**14**	**0**	**12**	**18**

III Semester

S. No.	Course Type/Code	Subject	Teaching Scheme			Credits
1	Prog. Specific Elective	a) Detection & Estimation Theory b) Advanced Digital Signal Processing c) Coding Theory and Applications	3	0	0	3
2	**Open Elective**	a) BusinessAnalytics b) IndustrialSafety c) OperationsResearch d) Cost Management of EngineeringProjects e) CompositeMaterials f) Waste toEnergy	3	0	0	3
3	Dissertation	Dissertation Phase – I	0	0	20	10
	Total		6	0	20	16

IV Semester

S. No.	Course Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	Dissertation	Dissertation Phase – II	--	--	32	16
	Total Credits		--	--	32	16

Total Credits: 18+18+16+16 = 68

Audit course 1 & 2

1. English for Research PaperWriting
2. DisasterManagement
3. Sanskrit for TechnicalKnowledge
4. ValueEducation
5. Constitution of India
6. PedagogyStudies
7. Stress Management byYoga
8. Personality Development through Life Enlightenment Skills.

Director (I/C)
Academic Planning
JNTUK Kakinada

Suggestions given by Board Members

1. For mini project append following define scope, tools and methodologies to be used , expected results. This can be included as part of presentation.
2. For DECE, DECS, ECE : Wireless Communications lab experiments can be done based on simulations in MATLAB.
3. Where ever possible for internal examinations /experimental questions can be evaluated based on the results.

   By adopting AICTE model curriculum, we here to ensure evaluation guide lines for project and other course as per our JNTUK norms.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE M.Tech ECE

Digital System & Computer Electronics (DSCE)

Programme

(Applicable for batches admitted from 2019-2020)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

I Semester

S. No.	Course Type/Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Core 1	VLSI Technology and Design	3	0	0	3
2	Core 2	Digital Data Communications	3	0	0	3
3	Prog. Specific Elective	**Elective I** a. Digital System Design b. Wireless Communications and Networks c. Internet Protocols	3	0	0	3
4	Prog. Specific Elective	**Elective II** a. Software Defined Radio b. Network Security and Cryptography c. Image & Video Processing	3	0	0	3
5	Lab 1	System Design & Data Communications Lab	0	0	4	2
6	Lab2	VLSI Technology Lab	0	0	4	2
7		Research Methodology and IPR	2	0	0	2
8	Aud 1	Audit Course 1	2	0	0	0
		Total	**16**	**0**	**8**	**18**

II Semester

S. No.	Course Type/Code	Name of the Subject	Teaching Scheme			Credits
			L	T	P	
1	Core 3	IoT and Applications	3	0	0	3
2	Core 4	DSP Processors & Architecture	3	0	0	3
3	Prog. Specific Elective	**Elective III** a. System On Chip Design b. Soft Computing Techniques c. Cyber Security	3	0	0	3
4	Prog. Specific Elective	**Elective IV** a. Embedded Real Time Operating Systems b. High Speed Networks c. EMI/EMC	3	0	0	3
5	Lab 1	Advanced Internet of Things (IoT) Lab	0	0	4	2
6	Lab2	DSP Processors & Architecture Lab	0	0	4	2
7	MP	Mini Project (Seminar)	0	0	4	2
8	Aud 2	Audit Course 2	2	0	0	0
		Total	**14**	**0**	**12**	**18**

III Semester

S. No.	Course Type/Code	Subject	Teaching Scheme			Credits
1	Prog. Specific Elective	**Elective V** a) Digital Design Using HDL b) CMOS Analog and Digital IC Design c) Advanced Computer Architecture	3	0	0	3
2	**Open Elective**	a) BusinessAnalytics b) IndustrialSafety c) OperationsResearch d) Cost Management of EngineeringProjects e) CompositeMaterials f) Waste toEnergy	3	0	0	3
3	Dissertation	Dissertation Phase – I	0	0	20	10
		Total	**6**	**0**	**20**	**16**

IV Semester

S.No.	Course Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	Dissertation	Dissertation Phase – II	--	--	32	16
	Total		--	--	32	**16**

Total Credits: 18+18+16+16 = 68

Audit course 1 & 2

1. English for Research PaperWriting
2. DisasterManagement
3. Sanskrit for TechnicalKnowledge
4. ValueEducation
5. Constitution of India
6. PedagogyStudies
7. Stress Management byYoga
8. Personality Development through Life Enlightenment Skills.

Director (I/c)
Academic Planning
JNTUK Kakinada

Suggestions given by Board Members

1. For mini project append following define scope, tools and methodologies to be used , expected results. This can be included as part of presentation.
2. For DSCE: Wireless Communications lab experiments can be done based on simulations in MATLAB.
3. Where ever possible for internal examinations /experimental questions can be evaluated based on the results.

   By adopting AICTE model curriculum, we here to ensure evaluation guide lines for project and other course as per our JNTUK norms.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE M.Tech ECE Common for

Communication Engineering & Signal Processing (CE&SP)
Communication & Signal Processing (CSP)

Programme

(Applicable for batches admitted from 2019-2020)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

I Semester

S. No.	Course Type/ Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Core 1	Advanced Digital Signal Processing	3	0	0	3
2	Core 2	Digital Image and Video Processing	3	0	0	3
3	Prog. Specific Elective	**Elective I** a. DSPArchitectures b. Statistical Signal Processing c. Cognitive Radio	3	0	0	3
4	Prog. Specific Elective	**Elective II** a. Adaptive Signal Processing b. Digital Data Communication c. Coding Theory & Applications	3	0	0	3
5	Lab 1	Advanced Digital Signal Processing Lab	0	0	4	2
6	Lab2	Digital Image and Video Processing Lab	0	0	4	2
7	MC	Research Methodology and IPR	2	0	0	2
8	Aud 1	Audit Course 1	2	0	0	0
		Total	**16**	**0**	**8**	**18**

II Semester

S. No.	Course Type/ Code	Name of the Subject	Teaching Scheme			Credits
			L	T	P	
1	Core 3	Pattern Recognition and Machine Learning	3	0	0	3
2	Core 4	Detection and Estimation Theory	3	0	0	3
3	Prog. Specific Elective	**Elective III** a. IOT and Applications b. Wireless Sensors Networks c. Soft Computing Techniques	3	0	0	3
4	Prog. Specific Elective	**Elective IV** a. Smart Antennas b. Biomedical Signal Processing c. Optical Networks	3	0	0	3
5	Lab 1	Pattern Recognition and Machine Learning Lab	0	0	4	2
6	Lab2	Detection and Estimation Theory Lab	0	0	4	2
7	MP	Mini Project (Seminar)	0	0	4	2
8	Aud 2	Audit Course 2	2	0	0	0
		Total	**14**	**0**	**12**	**18**

III Semester

S. No.	Course Type/Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	Prog. Specific Elective	**Elective-V** a. Optimization Techniques b. Modeling and Simulation Techniques c. Artificial Intelligence	3	0	0	3
2	**Open Elective**	a. Business Analytics b. Industrial Safety c. Operations Research d. Cost Management of Engineering Projects e. Composite Materials f. Waste to Energy	3	0	0	3
3	Dissertation	Dissertation Phase – I	0	0	20	10
	Total		**6**	**0**	**20**	**16**

IV Semester

S. No.	Course Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	Dissertation	Dissertation Phase – II	--	--	32	16
	Total		--	--	**32**	**16**

Total Credits: 18+18+16+16 = 68

Audit course 1 & 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills.

Director C/C
Academic Planning
JNTUK Kakinada

Suggestions given by Board Members

1.AICTE proposed Program Outcomes (POs) from 'a - e' may be adopted for CESP and CSP specializations

2.AICTE proposed syllabii for the course structure CESP and CSP are to be adopted

3. It is suggested to publish before final project dissertation in
   i) IEEE/SPRINGER conferences (mandatory)
   ii) Reputed journals (desirable)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE M.Tech ECE Common for

Systems & Signal Processing (SSP)
Digital Image Processing (DIP)

Programme

(Applicable for batches admitted from 2019-2020)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

I Semester

S. No.	Course Type/ Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Core 1	Advanced Digital Signal Processing	3	0	0	3
2	Core 2	Digital Image and Video Processing	3	0	0	3
3	Prog. Specific Elective	**Elective I** a. DSP Architectures b. Statistical Signal Processing c. Cognitive Radio	3	0	0	3
4	Prog. Specific Elective	**Elective II** a. Adaptive Signal Processing b. Computer Vision c. Coding Theory & Applications	3	0	0	3
5	Lab 1	Advanced Digital Signal Processing Lab	0	0	4	2
6	Lab2	Digital Image and Video Processing Lab	0	0	4	2
7	MC	Research Methodology and IPR	2	0	0	2
8	Aud 1	Audit Course 1	2	0	0	0
		Total	**16**	**0**	**8**	**18**

II Semester

S. No.	Course Type/ Code	Name of the Subject	Teaching Scheme			Credits
			L	T	P	
1	Core 3	Pattern Recognition and Machine Learning	3	0	0	3
2	Core 4	Detection and Estimation Theory	3	0	0	3
3	Prog. Specific Elective	**Elective III** a. IOT and Applications b. Wireless Sensors Networks c. Soft Computing Techniques	3	0	0	3
4	Prog. Specific Elective	**Elective IV** a. Audio/Vedio coding and compression b. Biomedical Signal Processing c. Optical Networks	3	0	0	3
5	Lab 1	Pattern Recognition and Machine Learning Lab	0	0	4	2
6	Lab2	Detection and Estimation Theory Lab	0	0	4	2
7	MP	Mini Project (Seminar)	0	0	4	2
8	Aud 2	Audit Course 2	2	0	0	0
		Total	**14**	**0**	**12**	**18**

III Semester

S. No.	Course Type/Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	Prog. Specific Elective	**Elective-V** a. Optimization Techniques b. Modeling and Simulation Techniques c. Artificial Intelligence	3	0	0	3
2	**Open Elective**	a. Business Analytics b. Industrial Safety c. Operations Research d. Cost Management of Engineering Projects e. Composite Materials f. Waste to Energy	3	0	0	3
3	Dissertation	Dissertation Phase – I	0	0	20	10
	Total		**6**	**0**	**20**	**16**

IV Semester

S. No.	Course Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	Dissertation	Dissertation Phase – II	--	--	32	16
	Total		--	--	**32**	**16**

Total Credits: 18+18+16+16 = 68

Audit course 1 & 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills.

Director (I/C)
Academic Planning
JNTUK Kakinada

Suggestions given by Board Members

1.AICTE proposed Program Outcomes (POs) from 'a - e' may be adopted for SSP,DIP specializations

2.AICTE proposed syllabii for the course structure SSP,DIP are to be adopted

3. It is suggested to publish before final project dissertation in

i) IEEE/SPRINGER conferences (mandatory)

ii) Reputed journals (desirable)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE M.Tech ECE

COMMUNICATION SYSTEMS (CS)

Programme

(Applicable for batches admitted from 2019-2020)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

I Semester

S. No.	Course Type/Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Core 1	Digital Data Communications	3	0	0	3
2	Core 2	Advanced Digital Signal Processing	3	0	0	3
3	Prog. Specific Elective	**Elective I** a. Radar Signal Processing b. RF Circuit Design c. Advanced Computer Networks	3	0	0	3
4	Prog. Specific Elective	**Elective II** a. Wireless LANs and PANs b. Mobile Computing Technologies c. Network Security & Cryptography	3	0	0	3
5	Lab 1	Data Communications Lab	0	0	4	2
6	Lab2	Advanced Digital Signal Processing Lab	0	0	4	2
7		Research Methodology and IPR	2	0	0	2
8	Aud 1	Audit Course 1	2	0	0	0
		Total	**16**	**0**	**8**	**18**

II Semester

S. No.	Course Type/Code	Name of the Subject	Teaching Scheme			Credits
			L	T	P	
1	Core 3	Wireless Communications and Networks	3	0	0	3
2	Core 4	Image and Video Processing	3	0	0	3
3	Prog. Specific Elective	**Elective III** a. Soft Computing Techniques b. Internet Protocols c. Cyber Security	3	0	0	3
4	Prog. Specific Elective	**Elective IV** a. Optical Networks b. DSP Processors and Architectures c. Radio and Navigational Aids	3	0	0	3
5	Lab 1	Advanced Communications Lab	0	0	4	2
6	Lab2	Advanced Image processing Lab	0	0	4	2
7	MP	Mini Project (Seminar)	0	0	4	2
8	Aud 2	Audit Course 2	2	0	0	0
		Total	**14**	**0**	**12**	**18**

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III Semester

S. No.	Course Type/Code	Subject	Teaching Scheme			Credits
1	Prog. Specific Elective	a) Detection & Estimation Theory b) Coding Theory and Applications c) Software Defined Radio	3	0	0	3
2	**Open Elective**	a) Business Analytics b) Industrial Safety c) Operations Research d) Cost Management of EngineeringProjects e) Composite Materials f) Waste to Energy	3	0	0	3
3	Dissertation	Dissertation Phase – I	0	0	20	10
	Total		6	0	20	16

IV Semester

S. No.	Course Code	Subject	Teaching Scheme			Credits
			L	T	P	
1	Dissertation	Dissertation Phase – II	--	--	32	16
	Total		--	--	32	16

Total Credits: 18+18+16+16 = 68

Audit course 1 & 2

1. English for Research PaperWriting
2. DisasterManagement
3. Sanskrit for TechnicalKnowledge
4. ValueEducation
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills.

Director (i/c)
Academic Planning
JNTUK Kakinada

Suggestions given by Board Members

1. For mini project append following define scope, tools and methodologies to be used , expected results. This can be included as part of presentation.
2. For CS : Wireless Communications lab experiments can be done based on simulations in MATLAB.
3. Where ever possible for internal examinations /experimental questions can be evaluated based on the results.

   By adopting AICTE model curriculum, we here to ensure evaluation guide lines for project and other course as per our JNTUK norms.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE M.Tech ECE

Embedded System (ES) Programme

(Applicable for batches admitted from 2019-2020)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

I-SEMESTER

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PC	Embedded System Design			3	0	0	3
2	PC	Microcontrollers and Programmable Digital Signal Processors			3	0	0	3
3	PE	1. Digital Signal and Image Processing 2. Parallel Processing 3. VLSI signal processing			3	0	0	3
4	PE	1. Programming Languages for Embedded Systems 2. System Design with Embedded Linux 3.CAD of Digital System			3	0	0	3
5		Research methodology and IPR			2	0	0	2
6	Lab 1	Embedded System Design Lab(using Embedded-C)			0	0	4	2
7	Lab 2	Microcontrollers and Programmable Digital Signal Processors Lab			0	0	4	2
8	Aud 1	Audit course-1			2	0	0	0
				Total				18

II-SEMESTER

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PC	Digital System Design			3	0	0	3
2	PC	Real Time Operating Systems			3	0	0	3
3	PE	1. Memory Architectures 2. SoC Design 3. Sensors &Actuators			3	0	0	3
4	PE	1.Communication Buses and Interfaces 2.Network Security and Cryptography 3.Physical design automation			3	0	0	3
5	Lab 1	RTOS Lab			0	0	4	2
6	Lab 2	Digital System Design Lab			0	0	4	2
7	MP	Mini Project			0	0	4	2
8	Aud 2	Audit Course – 2			2	0	0	0
				Total				18

*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

III-Semester*

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PE	1.IOT and its Applications 2.Hardware Software co-design 3.Artificial Intelligence			3	0	0	3
2	OE	1. Business Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of Engineering Projects 5. Composite Materials 6. Waste to Energy			3	0	0	3
3	Dissertation	Dissertation Phase -I /Industrial Project **(to be continued and evaluated next semester)**			0	0	20	10#
				Total				16

#Evaluated and Displayed in IV Sem Marks list.

*Students going for Industrial Project/Thesis will complete these courses through MOOCs

IV-Semester

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	Dissertation	Project/ DissertationPhase-II **(continued from III semester)**			0	0	32	16
				Total				16

Audit Course 1& 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills

Suggestions given by Board Members:

1. AICTE proposed Program Outcomes (POs) from 'a - e' may be adopted for ES specialization
2. AICTE proposed syllabii for the course structure ES are to be adopted
3. It is suggested to publish before final project dissertation in
   i) IEEE/SPRINGER conferences (mandatory)
   ii) Reputed journals (desirable)

Director (i/c)
Academic Planning
JNTUK Kakinada

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE M.Tech ECE
VLSI& Embedded System, Embedded System &VLSI, VLSI Design& Embedded System, Embedded System& VLSI Design Programme

(Applicable for batches admitted from 2019-2020)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

I-Semester

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PC	RTL Simulation and Synthesis with PLDs			3	0	0	3
2	PC	Microcontrollers and ProgrammableDigital Signal Processors			3	0	0	3
3	PE	1. Digital Signal and Image Processing 2. Parallel Processing 3. VLSI signal processing			3	0	0	3
4	PE	1. Programming Languages for Embedded Systems 2. System Design with Embedded Linux 3.CAD of Digital System			3	0	0	3
5		Research methodology and IPR			2	0	0	2
6	Lab 1	RTL Simulation and Synthesis withPLDs Lab			0	0	4	2
7	Lab 2	Microcontrollers and Programmable Digital Signal Processors Lab			0	0	4	2
8	Aud 1	Audit course-I			2	0	0	0
				Total				18

II -Semester

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PC	Analog and Digital CMOS VLSI Design			3	0	0	3
2	PC	VLSI Design Verification and Testing			3	0	0	3
3	PE	1. Memory Architectures 2. SoC Design 3.Low power VLSI Design			3	0	0	3
4	PE	1.Communication Buses and Interfaces 2.Network Security and Cryptography 3.Physical design automation			3	0	0	3
5	Lab 1	Analog and Digital CMOS VLSI Design Lab			0	0	4	2
6	Lab 2	VLSI Design Verification and Testing Lab			0	0	4	2
7	MP	Mini Project			0	0	4	2
8	Aud 2	Audit Course – 2			2	0	0	0
				Total				18

*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

III-SEMESTER

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PE	1.IOT and its Applications 2.Hardware Software co-design 3.Artificial Intelligence			3	0	0	3
2	OE	1. Business Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of Engineering Projects 5. Composite Materials 6. Waste to Energy			3	0	0	3
3	Dissertation	Dissertation Phase -I /Industrial Project **(to be continued and evaluated next semester)**			0	0	20	10#
				Total				16

#Evaluated and Displayed in IV Sem Marks list.

*Students going for Industrial Project/Thesis will complete these courses through MOOCs

IV -SEMESTER

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	Dissertation	Project/ Dissertation Phase-II **(continued from III semester)**			0	0	32	16
				Total				16

Audit Course 1& 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills

Suggestions given by Board Members:

1. AICTE proposed Program Outcomes (POs) from 'a - e' may be adopted for ESVLSI,VLSIES,VLSIDES,ESVLSID specialization
2. AICTE proposed syllabii for the course structure ESVLSI,VLSIES,VLSIDES,ESVLSID are to be adopted
3. It is suggested to publish before final project dissertation in
   i) IEEE/SPRINGER conferences (mandatory)
   ii) Reputed journals (desirable)

Director (I/c)
Academic Planning
JNTUK Kakinada

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE M.Tech ECE
VLSI, VLSI Design, VLSI System Design,
VLSI Micro-Electronic Programme

(Applicable for batches admitted from 2019-2020)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

I -SEMESTER

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PC	CMOS Analog IC Design			3	0	0	3
2	PC	CMOS Digital IC design			3	0	0	3
3	PE	1. VLSI Technology 2. Nanomaterials and Nanotechnology 3. MEMS Technology			3	0	0	3
4	PE	1. Device Modeling 2.Nano-electronics 3.Photonics			3	0	0	3
5		Research methodology and IPR			2	0	0	2
6	Lab 1	CMOS Analog IC Design Lab			0	0	4	2
7	Lab 2	CMOS Digital IC Design Lab			0	0	4	2
8	Aud 1	Audit course-1			2	0	0	0
				Total				18

II -SEMESTER

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PC	Mixed Signal & RF IC Design			3	0	0	3
2	PC	Physical Design Automation			3	0	0	3
3	PE	1. Design For Testability 2. IOT & its Applications 3. VLSI Signal Processing			3	0	0	3
4	PE	1.Network Security & Cryptography 2.Microcontrollers & programmable Digital Signal Processors 3. Low Power VLSI Design			3	0	0	3
5	Lab 1	Mixed Signal IC Design Lab			0	0	4	2
6	Lab 2	Physical Design Automation Lab			0	0	4	2
7	MP	Mini Project			0	0	4	2
8	Aud 2	Audit Course – 2			2	0	0	0
				Total				18

*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

III-Semester

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	PE	1.Scripting Languages for VLSI 2. Digital System Design & Verification 3.Hardware Software co-design 4.Artificial Intelligence			3	0	0	3
2	OE	1. Business Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of Engineering Projects 5. Composite Materials 6. Waste to Energy			3	0	0	3
3	Dissertation	Dissertation Phase -I /Industrial Project **(to be continued and evaluated next semester)**			0	0	20	10#
				Total				16

#Evaluated and Displayed in IV Sem Marks list.

*Students going for Industrial Project/Thesis will complete these courses through MOOCs

IV-Semester

S.No	Course No	Course Name	P.Os	Category	L	T	P	Credits
1	Dissertation	Project/ DissertationPhase-II **(continued from III semester)**			0	0	32	16
				Total				16

Audit Course 1& 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills

Suggestions given by Board Members:

1. AICTE proposed Program Outcomes (POs) from 'a - e' may be adopted for VLSI,VLSID,VLSISD,VLSI ME specialization
2. AICTE proposed syllabii for the course structure VLSI,VLSID,VLSISD,VLSI ME are to be adopted
3. It is suggested to publish before final project dissertation in
   i) IEEE/SPRINGER conferences (mandatory)
   ii) Reputed journals (desirable)

Director C/c
Academic Planning
JNTUK Kakinada